AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [35] with the following amended paragraph:

[35] FIG. 2B is a diagram of an exemplary system at time T2 that may be utilized for monitoring a set of semaphore registers using a limited-width test bus, in accordance with an embodiment of the invention. While any one time instant is indicative of which hardware resources are in use, only monitoring changes can provide sufficient information to determine the ID number of the software thread using the hardware resource. Referring to FIG. 2B, at time instant T2, a software thread has taken ownership of the hardware resource corresponding to semaphore register 204 labeled Register 1. The software thread has written its ID number into the register which change the value of 3 register bit locations 216 in semaphore register 204 labeled Register 1. The output of the multiple-input OR gate 206 labeled OR-1 has changed from a value of logic 0 to a value of logic 1 to indicate that the corresponding hardware resource is now in use. The outputs of multiple-input XOR gates 206 labeled XOR-6, XOR-4, and XOR-1 have also changed values. Because the previous value in semaphore register 204 labeled Register 1 was logic 0, and since only [[ ]]one semaphore register 204 can change at a time according to the semaphore protocol assumptions, the changes in the outputs of multiple-input XOR gates 206 labeled XOR-6, XOR-4, and XOR-1 indicate that the corresponding register bit locations 214 have changed from logic 0 to logic 1. Assuming all the previous values of all the registers are known, then knowing which bits of which semaphore register ~~205~~ 204 have changed may be enough information to update the known values of the registers. The assumption that the previous values of all the semaphore registers 204 are known may be made because the semaphore registers 204 initially started off in their reset state.

Please replace paragraph [36] with the following amended paragraph:

[36] FIG. 2C is a diagram of an exemplary system that may be utilized for monitoring blocks of semaphore registers using a limited-width test bus, in accordance with an embodiment of the invention. In another embodiment of the invention, when the semaphore protocol requires that the reset state or default value of the semaphore registers 204 be logic 1, then the multiple-input OR gates 206 in FIG. 2A and FIG. 2B may be replaced by a multiple-input AND gate 218. In this instance semaphore register 204 labeled Register 1 is set to logic 1. All the bits of semaphore register 204 labeled Register 1 are coupled to the multiple-input AND gate 218 labeled AND-1. The output of the multiple-input AND gate ~~216~~ 218 labeled AND-1 is logic 1, which indicates that the hardware resource corresponding to the semaphore register 204 labeled Register 1 is available. A zero value would indicate that the hardware resource is in use. The value of the multiple-input AND gate 218 labeled AND-1 is monitored by SRBT 210 and therefore by the LWTB 202. Similarly, the outputs of all other multiple-input AND gates 218 are monitored by SRBT 210 and therefore by the LWTB 202.